Amendments to the Specification

Please **add** the following paragraph at page 1, line 5:

-- This application claims the benefit, under 35 U.S.C. § 365 of International Application PCT/EP02/14711, filed December 23, 2002, which was published in accordance with PCT Article 21(2) on July 17, 2003 in English and which claims the benefit of German patent application No. 10200990.2, filed January 14, 2002. --

Please **replace** the following paragraph beginning at page 1, line 10 with the following **rewritten** paragraph:

-- The invention relates to a method for storing video signals. ~~with the aid of a random access memory (SDRAM) that is operated synchronously during writing and reading, there being connected downstream of the random access memory a further memory (FIFO) with different frequencies for writing and reading.~~ --

Please **replace** the following paragraph beginning at page 1, line 20, with the following **rewritten** paragraph:

-- Television equipment and systems often require storage of video signals, and reading and writing are to be performed with different clocks. This is the case for example in film scanners and in synchronising devices. Examples of memory ~~Memory~~ modules in which reading can be effected with a different clock from writing ~~are~~ include so-called FIFOs (First-In First-Out) ~~for example~~. The latter have the disadvantage however, that they are available for the large capacity required for the abovementioned purposes only with a considerable outlay. Moreover, the maintenance of the temporal sequence of the signal, that is to say of the pixels, which is provided in the case of FIFOs considerably restricts their use. Although random access memories (RAMs) are more advantageous in this respect, the addressing and changeover between writing and reading operation reduces the speed.

Please **replace** the following paragraphs beginning at page 2, line 4 and ending at page 4, line 9, with the following **new** paragraph:

-- An embodiment of the invention provides a method for storing video signals at a first rate and reading the stored video signals at a second rate. According to an embodiment of the method, the video signals to be stored are compressed. The compressed video signals are stored in a memory at a first rate. The compressed video signals a read from the memory into a buffer at the first rate. The video signals stored in the buffer are read from the buffer at a second rate such that the video signals are decompressed. with the aid of a random access memory ~~(SDRAM)~~ that is operated synchronously during writing and reading, there being connected downstream of the random access memory a further memory ~~(FIFO)~~ with different frequencies for writing and reading, the video signals to be stored are divided into a plurality of parallel data streams. The data streams are time-compressed in such a way that the compressed data streams take up only a part of a predetermined write-read cycle for the random access memory. Data streams read from the random access memory are conducted via the further memory and combined to form video signals. --

Please **delete** the paragraph beginning on page 4, line 13:

~~-- An exemplary embodiment of the invention is illustrated in the drawing using a plurality of figures and is explained in more detail in the description below. In the figures: --~~

Please **replace** the following paragraph beginning at page 4, line 30 with the following **rewritten** paragraph:

--Detailed Description of the ~~exemplary embodiments~~ Drawings --

Please add the following new paragraphs after the paragraph ending on line 30 at page 4:

-- A method according to an embodiment of the invention operates such that video signals to be stored are divided into a plurality of parallel data

streams. The data streams are time-compressed in such a way that the compressed data streams take up only a part of a predetermined write-read cycle for the memory. In one embodiment of the invention, the memory is a Random Access Memory, for example, an SDRAM. The data streams read from the memory are conducted via a second memory, according to one embodiment, a buffer memory. The data streams are combined, i.e., decompressed, to form video signals. In an embodiment of the invention, the data streams are provided to a multiplexer for re-combining or decompressing.

The method according to the invention enables rapid reading and writing, so that even video signals with very high bit rates can be stored. Moreover, SDRAMs with large capacities can be obtained at low cost. In the case of the method according to the invention, the rapid writing and reading is made possible in particular by virtue of the fact that not every memory location need be addressed individually, rather only one bank address is used for a data block comprising 512 pixels, for example, which are read again in the same sequence. Nevertheless, the method according to the invention is extremely flexible and enables the video signals to be read in a manner largely independent of the clock and the structure (number of pixels, number of lines, interline or progressive) of the video signals supplied.

In order to enable reading of the video signals faster than writing, the method according to the invention may provide for the write-read cycle to comprise a write period and at least one read period. In this case, it has proved to be advantageous if the write-read cycle comprises a write period and three read periods.

An advantageous refinement of the method according to the invention consists in the fact that the write or read periods in each case contain, prior to the writing or reading, respectively, control time segments for setting the random access memory for writing or reading, respectively, and, after the write or read periods, respectively, control time segments for terminating the writing or reading, respectively. In said time segments, all the commands required for the subsequent writing or reading are fed to the random access memories.

In this case, it may furthermore be provided that the random access memory is furthermore refreshed in the time segments. This refinement can be developed such that in the control time segments preceding the writing or reading, the following code sequence is fed to the random access memory: NOPs, PALL, NOPs, REF, ACTV, ACTV, NOPs.

By virtue of the fact that the control time segments contain defined signals - in contrast to the continuously changing video data - the signals in the control time segments can readily be utilised for the synchronisation of digital measurement and test devices.

In a method embodied in practice, it was furthermore provided that in the control time segments after writing or reading, the following code sequence is fed to the random access memory: BST, PALL, REF, NOPs.

Details of these code sequences depend on the respective embodiments of the SDRAMs.

The division of the video signals (demultiplex) may be chosen differently depending on requirements made of speed, made of quantity of video data to be stored, and depending on the SDRAM used. In a method carried out in practice, it has proved expedient for the video signals to be divided pixel by pixel.--